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Free range vhdl - Greg Stitt, University of Florida

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In VHDL, a design consists at a minimum of an entity which describes the interface and an architecture which contains the actual implementation.

VHDL - Wikipedia

Circuit Design with VHDL, 1st edition, Volnei A. Pedroni, MIT Press, 2004 Selected Exercise Solutions

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Virtex-4 FPGA User Guide www.xilinx.com UG070 (v2.6) December 1, 2008 Xilinx is disclosing this user guide, manual, release note, and/ or specification (the ...

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Verilog - Wikipedia

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